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(54) Transmitter power amplifier control

(57) A circuit for controlling the gain of a power amplifier for a transmitter. The circuit comprises means for monitoring the input to the power amplifier. Means also monitors the output of the power amplifier. There is also means for detecting and comparing the amplitude envelopes of the two monitored signals to produce a signal without any envelope content. Further means varies the gain of the power amplifier dependent upon the output of the comparator and a low pass integrating filter.

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Description

[0001] This invention relates to the control of a power amplifier for use in mobile telecommunication systems such as mobile telephones.

[0002] The need to control the power amplifiers associated with the transmitting antennas in such systems is well known, and numerous different circuits for controlling such power amplifiers have been proposed previously. For example, numerous different types of control circuitry have been proposed for controlling power transmitter used in the GSM mobile telephony standard, and one such circuit is described below that has particular benefits when employed in a GSM system for data in the GMSK format that is well known within that system.

[0003] However, in recent times there has been a proposal to use a different format in the GSM system, that known as EDGE (enhanced data GSM environment). This format, which is described in the publications, GSM/EDGE: device characterisation for RF power amplifier. Jean Christophe Nanan. Motorola Toulouse. Microwave engineering Europe March 2000, Understanding Offset 8-PSK modulation for GSM EDGE. Ashkan Mashhour, Nokia Telecommations, Camberley, UK. Microwave Journal. October 1999, and GSM 3GPP TS 05.05 v 8.8.0 (2001-01), has certain advantages over the GMSK format in that it enables a higher data transmission rate and in that it makes more efficient use of the spectrum available for GSM transmissions. However, signals produced in accordance with this format have a number of characteristics which differ from those produced in accordance with the GMSK format. One characteristic is that of variable amplitude envelope. GMSK signals have a constant amplitude envelope which results in a straightforward control concept when monitoring the output of a transmitter power amplifier for such signals, as is described below. However, EDGE signals have a variable envelope that makes such an approach to power amplifier control unacceptable and very likely to introduce large errors and discrepancies into the signal that which will largely reduce transmission accuracy.

[0004] Accordingly, the present invention seeks to provide control circuitry for use with a power amplifier for data signals with non-constant amplitude envelope that overcomes the problems associated with current known power amplifier circuitry.

[0005] According to the present invention there is provided a circuit for controlling the gain of a power amplifier for a transmitter, the circuit comprising:

means for monitoring the input to the power amplifier;
means for monitoring the output of the power amplifier;
means for detecting the amplitude envelope of the two monitored signals to produce envelope signals for each;
a comparator for comparing the envelope signals; and
means for varying the gain of the power amplifier dependent upon the output of the comparator.

[0006] The circuit may further comprise the power amplifier and may also comprise an antenna. The circuit may further comprise a transmitter circuit for producing an input to the power amplifier in accordance with the EDGE format.

[0007] The means for detecting the envelope may comprise a diode. In this case, the means for monitoring the output of the power amplifier may comprise an attenuator and a variable gain amplifier, the variable gain amplifier having its gain controlled by the output of a ramp digital-to-analogue converter. In this case, the ramp digital-to-analogue converter may provide the reference for power output level.

[0008] Alternatively, the means for monitoring the input and output signals for the power amplifier may comprise respective attenuators for each signal in combination with respective log amplifiers. In this case the comparison means comprises a first comparator for providing a comparison between the output of the two log amplifiers, followed by a second comparator which compares the output of the first comparator with the output from a ramp digital-to-analogue converter. So that this second comparator compares effectively two gains. The ramp digital-to-analogue converter provides the reference gain and the first comparator provides the gain of the power amplifier. If there is a difference between the two gains, an error is generated, integrated and then applied to the gain control input of the power amplifier.

[0009] With the present invention, signals coming from the output and input of the power amplifier will be detected by the log amplifiers and the first comparator will compute a voltage difference representing the difference in dB between the two signal levels, so that this difference can be interpreted as the RF gain of the power amplifier. When the EDGE data format is used, the signals produced by the log amplifiers will vary in amplitude reflecting the non-constant envelope nature of the EDGE signals. However, as the first comparator computes the difference in dB between the signal levels, the non-constant envelope will be removed from the difference computation. So, even signals with variable envelope, such as signals in accordance with the EDGE format, can be monitored to provide variable gain control of the power amplifier.

[0010] Examples of the present invention will now be described with reference to the accompanying drawings, in which:

Figure 1 is a schematic circuit diagram of a prior art amplifier control circuit;
Figure 2 is a schematic circuit diagram of a first example of the present invention; and
Figure 3 is a schematic circuit diagram of a second

example of the present invention.

[0011] Referring to Figure 1, a known automatic power control (APC) circuit for a power amplifier 1 is shown. Also shown in Figure 1 is the associated circuitry for use with a power amplifier 1 in a mobile telecommunications device such as a mobile telephone.

[0012] In this circuit a signal to be transmitted is generated by a transmitter circuitry 2 from I and Q signals. The signal to be transmitted is then passed through a high frequency range cut-off band pass filter 3 to the power amplifier 1. The signal to be transmitted is then amplified by the power amplifier 1 and forwarded to an antenna 4 for transmission. In the prior art the output level of the power amplifier 1 is attenuated, detected and compared with the output of a fixed digital-to-analogue converter 5. The resulting error is used to adjust the desired transmission level in accordance with the reference provided by the digital-to analog converter. Such an APC circuit controls the power ramping of the power amplifier and ensures that temperature and supply voltage variations do not affect the output level of the power amplifier 1 during the active part of the burst signal.

[0013] This arrangement works well for a signal with a constant envelope, such as a GMSK format signal, but for a signal in which the amplitude envelope varies (such as an EDGE signal) it tends to reduce the dynamic of the envelope, affecting the output signal. This is because the control band-width must be designed for ramping of the power from the output of the ramp DAC 7. In practice this means that the output level needs to track the ramping shape over less than 20 ms, so the loop has a bandwidth of the order of 100 Khz. A control loop with this bandwidth will also provide, however, undesired compensation for amplitude envelope variations in an EDGE format signal, cutting out certain frequency components therefrom and reducing the signal's dynamic range.

[0014] Figure 2 is a schematic circuit diagram of a first example of an APC circuit according to the present invention. Components that correspond to those in figure 1 are numbered identically. In this circuit the input to the power amplifier 1 is a signal accordance with the EDGE format. This input signal is monitored and fed through a first envelope detecting diode 8 so that it can be provided to a comparator 9. The output of the power amplifier 1 is also monitored, attenuated, and then fed through a variable gain amplifier 10, the output of the variable gain amplifier 10 is then fed through a second envelope-detecting diode 11 and fed to the second input of the comparator 9. The gain of the variable gain amplifier 10 is controlled by the output of a ramp digital-to-analogue converter 7. Therefore the ramping signal from the ramp DAC 7 fixes the output level of the power amplifier as the envelope-detected signals must always remain the same. The output of the comparator 9 is then fed through an integrator 12 and the output used to control the gain of the power amplifier 1.

[0015] In this circuit the effect of amplitude envelope variation in the EDGE format signals is removed from the control loop. The error signal computed by the comparator will only reflect the gain variations due to supply voltage or temperature changes. This error signal is filtered by a low pass integrator 12 that fixes the control loop bandwidth to a an optimal value that guarantees stability over the required output power range, reduces the wideband noise level in the loop and follows the ramping signal with a reasonable accuracy.

[0016] Figure 3 shows a further example of the present invention. This may be used in certain circumstances because of limitations in the circuitry of figure 2. For example, the circuitry of figure 2 may need in many circumstances additional gain compensation after the comparator in order to stabilise the loop bandwidth at the optimal value during power ramping. Also, in the circuit of figure 2 the feedback path must be very linear over the whole dynamic range of the signal that is input to the power amplifier 1, and in the case of an edge format signal this means from -13.4dBm to +32.4dBm. Also the amplitude detectors must be very linear over at least the EDGE dynamic range of 16.8 dB. Furthermore, in the circuit of figure 2 there is a need to control carefully any wide band noise generated in the feedback path.

[0017] The alternative circuit of figure 3, in which components which correspond to those of the previous figures are numbered identically, employs a comparison of signal power to overcome the limitations of the circuit of figure 2. In this case, the input and output signals from the power amplifier 1 are monitored and attenuated by attenuators 13, 14 before being fed to log amplifiers 15, 16. The outputs of the log amplifiers 15,16 are then fed to comparison circuitry which comprises a first comparator 17, which provides an output signal which is indicative of the difference between the outputs of the log amplifiers 15,16. The comparator circuitry 17 then comprises a further comparator 18 which compares the output of the first comparator 17 with that of a ramp DAC 7. Again, the output of the comparator circuitry 17, 18 is fed through a low pass filter 12 before being used to control the gain of the power amplifier 1.

[0018] As already explained, by comparing the power of the input and output signals for the power amplifier 1, the envelope of the input signal and the output signal are removed from the comparison. With this circuitry the feedback loop that it provides is effectively providing a small-signal gain which varies as the derivative of a logarithmic function, so that the loop has maximum gain at low power levels and minimum gain at high power levels. These small signal gain variations are compensated by the non-linear nature of the gain control characteristics of the power amplifier. At low power, the power amplifier has a small small-signal-gain and at high power level, the power amplifier has a high small-signal gain. So that, in the end, the feedback loop bandwidth remains constant and stable over the power ramping range.

Claims

1. A circuit for controlling the gain of a power amplifier for a transmitter, the circuit comprising:

   means for monitoring the input to the power amplifier;
   means for monitoring the output of the power amplifier;
   means for detecting the amplitude envelopes of the two monitored signals to produce envelope detected signals for each;
   a comparator for comparing the envelopes of the signals; and
   means for varying the gain of the power amplifier with a special gain control input.

2. A circuit according to claim 1 further comprising a power amplifier.

3. A circuit according to claim 1 or claim 2, further comprising an antenna.

4. A circuit according to any of claims 1 to 3 further comprising a transmitter circuit for producing an input to the power amplifier in accordance with the EDGE format.

5. A circuit according to any preceding claim, where the means for detecting the envelope comprises diodes associated with the input and output signals of the power amplifier.

6. A circuit according to claim 5, wherein the means for monitoring the output of the power amplifier comprises an attenuator and a variable gain amplifier, the variable gain amplifier having its gain controlled by the output of a ramp digital-to- analogue converter.

7. A circuit according to claim 6, wherein the ramp digital-to-analogue converter provides a reference to the comparator.

8. A circuit according to any of claims 1 to 4, wherein the means for monitoring the input and output signals for the power amplifier comprises respective attenuators for each signal in combination with respective log amplifiers.

9. A circuit according to claim 8, wherein the comparison means comprises a first comparator for providing a comparison between the output of the two log amplifiers, and a second comparator which compares the output of the first comparator with the output from a ramp digital-to-analogue converter.

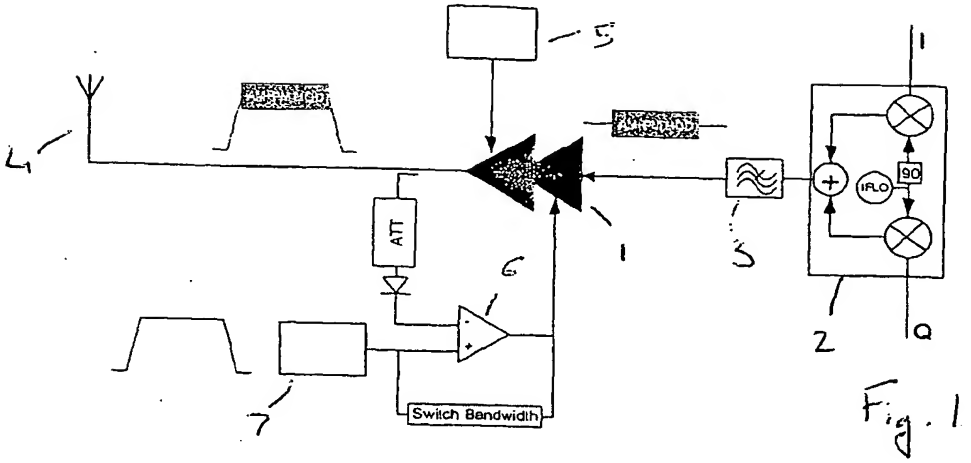

Fig. 1

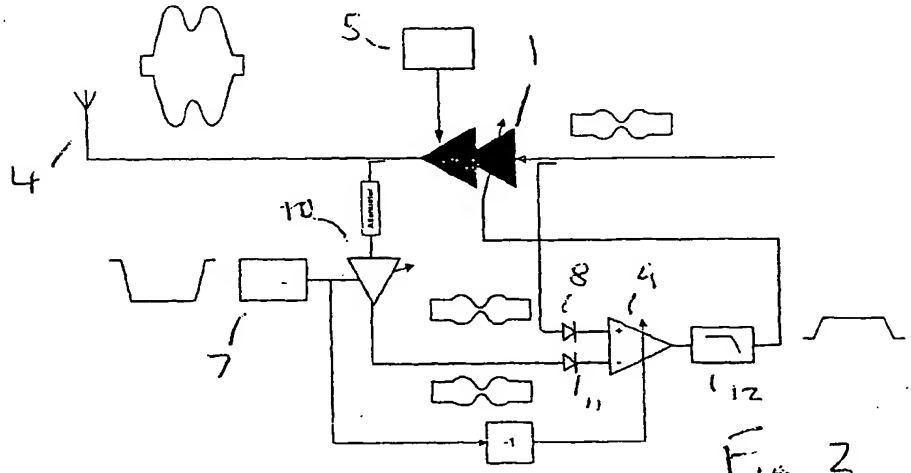

Fig. 2

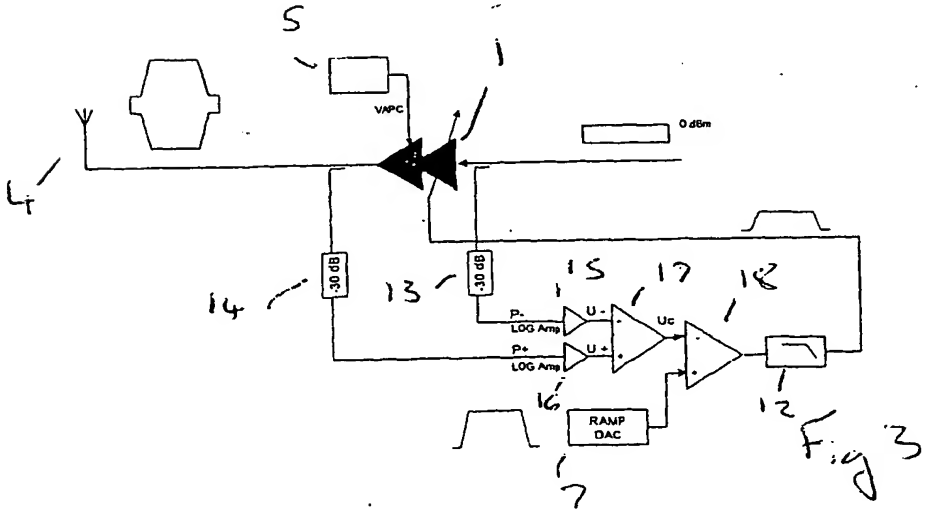

Fig. 3

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EUROPEAN SEARCH REPORT

Application Number
EP 01 30 6052

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
A	WO 01 03292 A (NOKIA NETWORKS OY ;TRAN KIM ANH (US); WEY CHIA SAM (US); NEITINIEM) 11 January 2001 (2001-01-11) * page 6, line 12 - column 7, line 21; figure 3 *	1	H03G3/30
A	WO 01 10013 A (MECK RONALD A ;TROPIAN INC (US); SANDER WENDELL (US); MCCUNE EARL) 8 February 2001 (2001-02-08) * page 15, paragraph 2 - page 16, paragraph 1 *	1	
A	US 6 008 698 A (DACUS FARRON L ET AL) 28 December 1999 (1999-12-28) * column 14, line 20 - line 42; figure 12 *	1	

TECHNICAL FIELDS SEARCHED (Int.Cl.7)

H03G

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	21 December 2001	Blaas, D-L

CATEGORY OF CITED DOCUMENTS

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ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO. EP 01 30 6052

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report. The members are as contained in the European Patent Office EDP file on
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